What is claimed is:

1. A semiconductor device, comprising:

an active area formed in a semiconductor substrate; and

an isolation structure comprising at least one dielectric material disposed within a trench which extends into said semiconductor substrate, wherein said isolation structure substantially surrounds said active area, and wherein at least a portion of said isolation structure is adapted to modify stresses incurred on said active area.

2. The semiconductor device of claim 1, wherein said active area further comprises nMOS device components including an n-type source region, an n-type drain region, and a gate structure disposed adjacent said active area between said n-type source region and said n-type drain region.

3. The semiconductor device of claim 2, wherein said isolation structure comprises a low-modulus, dielectric material disposed within said at least a portion of said trench.

4. The semiconductor device of claim 2, wherein said isolation structure comprises a tensile stress-inducing, dielectric material disposed within said at least a portion of said trench.

5. The semiconductor device of claim 2, wherein said active area includes a width and wherein said isolation structure comprises at least a portion of said trench having a depth such that an aspect ratio of said trench portion depth to said active area width is greater than about 0.5.

6. The semiconductor device of claim 5, wherein said isolation structure comprises a low-modulus, dielectric material disposed within said at least a portion of said trench.

7. The semiconductor device of claim 5, wherein said isolation structure comprises a tensile stress-inducing, dielectric material disposed within said at least a portion of said trench.

8. The semiconductor device of claim 1, wherein said active area further comprises pMOS device components including a p-type source region, a p-type drain region, and a gate structure disposed adjacent said active area between said p-type source region and said p-type drain region.

9. The semiconductor device of claim 8, wherein said isolation structure comprises a low-modulus, dielectric material disposed within said at least a portion of said trench parallel to a channel current direction of the pMOS device components.

10. The semiconductor device of claim 9, wherein said isolation structure comprises a high-modulus, dielectric material disposed within said at least a portion of said trench perpendicular to the channel current direction of the pMOS device components.

11. The semiconductor device of claim 8, wherein said isolation structure comprises a low-modulus, dielectric material disposed within said at least a portion of said trench perpendicular to a channel current direction of the pMOS device components.

12. The semiconductor device of claim 11, wherein said isolation structure comprises a high-modulus, dielectric material disposed within said at least a portion of said trench parallel to the channel current direction of the pMOS device components.

13. The semiconductor device of claim 8, wherein said isolation structure comprises a tensile stress-inducing, dielectric material disposed within said at least a portion of said trench parallel to the channel current direction of the pMOS device components.

14. The semiconductor device of claim 8, wherein said isolation structure comprises a compressive stress-inducing, dielectric material disposed within said at least a portion of said trench perpendicular to the channel current direction of the pMOS device components.

15. The semiconductor device of claim 8, wherein said isolation structure comprises at least a portion of said trench parallel to a channel current direction of the pMOS device components having a depth wherein said active area includes a width and wherein said isolation structure comprises at least a portion of said trench parallel to a channel current direction of the pMOS device having a depth such that an aspect ratio of said trench portion depth to said active area width is greater than about 0.5.

16. The semiconductor device of claim 15, wherein said isolation structure comprises a low-modulus, dielectric material disposed within said at least a portion of said trench parallel to the channel current direction.

17. The semiconductor device of claim 15, wherein said isolation structure comprises a tensile stress-inducing, dielectric material disposed within said at least a portion of said trench parallel to the channel current direction.

18. The semiconductor device of claim 15, wherein said isolation structure comprises a high-modulus, dielectric material disposed within said at least a portion of said trench perpendicular to the channel current direction of the pMOS device components.

19. The semiconductor device of claim 15, wherein said isolation structure comprises a compressive stress-inducing, dielectric material disposed within said at least a portion of said trench perpendicular to the channel current direction of the pMOS device components.

20. The semiconductor device of claim 8, wherein said active area includes a width and wherein said isolation structure comprises at least a portion of said trench perpendicular to a channel current direction of the pMOS device components having a depth such that an aspect ratio of said trench portion depth to said active area width is greater than about 0.5.

21. The semiconductor device of claim 20, wherein said isolation structure comprises a low-modulus, dielectric material disposed within said at least a portion of said trench perpendicular to the channel current direction of the pMOS device components.

22. The semiconductor device of claim 20, wherein said isolation structure comprises a compressive stress-inducing, dielectric material disposed within said at least a portion of said trench perpendicular to the channel current direction of the pMOS device components.

23. The semiconductor device of claim 20, wherein said isolation structure comprises a high-modulus, dielectric material disposed within said at least a portion of said trench parallel to the channel current direction of the pMOS device components.

24. The semiconductor device of claim 20, wherein said isolation structure comprises a tensile stress-inducing, dielectric material disposed within said at least a portion of said trench parallel to the channel current direction of the pMOS device components.

25. A method of forming an stress modifying isolation structure, comprising:

forming a trench in said semiconductor substrate to substantially surround an active area of a semiconductor substrate; and

disposing at least one stress-modifying, dielectric material within at least a portion said trench.

26. The method of claim 25, wherein said disposing said at least one stress-modifying, dielectric material within said at least a portion of said trench comprises disposing a low-modulus, dielectric material within said at least a portion of said trench.

27. The method of claim 25, wherein said disposing said at least one stress-modifying, dielectric material within said at least a portion of said trench comprises disposing a tensile stress-inducing, dielectric material disposed within said at least a portion of said trench.

28. The method of claim 25, wherein said disposing said at least one stress-modifying, dielectric material within said at least a portion of said trench comprises disposing a high-modulus, dielectric material within said at least a portion of said trench.

29. The method of claim 28, wherein said disposing said at least one stress-modifying, dielectric material within said at least said portion of said trench comprises disposing a compressive stress-inducing, dielectric material within said at least said portion of said trench.

30. A method of forming an stress modifying isolation structure, comprising:

forming a trench in said semiconductor substrate to substantially surround an active area, wherein said active area includes a width and wherein at least a portion of said trench includes a depth such that an aspect ratio of said trench portion depth to said active area width is greater than about 0.5; and

disposing at least one dielectric material within at least a portion of said trench.

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